

## CLAIMS

Having thus described our invention in detail, what we claim as new, and desired to secure by the Letters Patent is:

1. A method of forming an interconnect structure including a patterned anti-fuse dielectric layer formed on surface of a substrate, said method comprising the steps of:
  - (a) forming an anti-fuse dielectric layer on a surface of a substrate, said substrate having a first level of electrically conductive features;
  - (b) forming an interlevel dielectric layer on said anti-fuse dielectric layer;
  - (c) forming vias in said interlevel dielectric layer exposing portions of said anti-fuse dielectric layer that overlay said first level of electrically conductive features;
  - (d) forming a wire level mask on said interlevel dielectric layer, wherein at least of one of said vias and a portion of said interlevel dielectric layer are left exposed;
  - (e) etching exposed portions of said anti-fuse dielectric layer from said exposed vias, wherein during said etching a portion of said exposed interlevel dielectric layer is removed so as to form a space wherein a second level of

27 electrically conductive features will be subsequently  
28 formed;

29  
30 (f) stripping said wire level mask; and

31  
32 (g) filling said vias including said spaces with a  
33 conductive material, whereby said second level of  
34 electrically conductive features is formed.

1 2. The method of Claim 1 wherein said first level of  
2 electrically conductive features is formed by a single or  
3 dual damascene process.

1 3. The method of Claim 1 wherein step (a) includes a  
2 deposition process selected from the group consisting of  
3 CVD, plasma-assisted CVD, sputtering and evaporation.

1 4. The method of Claim 1 wherein said anti-fuse  
2 dielectric has a thickness of from about 2 to about 200  
3 nm.

1 5. The method of Claim 4 wherein said anti-fuse  
2 dielectric has a thickness of from about 5 to about 10  
3 nm.

1 6. The method of Claim 1 wherein said anti-fuse  
2 dielectric is a dielectric material selected from the  
3 group consisting of  $\text{SiO}_2$ ,  $\text{Si}_3\text{N}_4$ , Si oxynitrides, amorphous  
4 Si, amorphous C, H-containing dielectrics, carbon,  
5 germanium, selenium, compound semiconductors, ceramics  
6 and anti-reflective coatings.

1 7. The method of Claim 6 wherein said anti-reflective  
2 coating is a silicon oxynitride.

1 8. The method of Claim 1 wherein step (b) includes a  
2 deposition process and, optionally, a planarization  
3 process.

1 9. The method of Claim 8 wherein said deposition process  
2 is selected from the group consisting of chemical vapor  
3 deposition (CVD), plasma-assisted CVD, sputtering,  
4 plating and evaporation.

1 10. The method of Claim 8 wherein said optional  
2 planarization process includes chemical-mechanical  
3 polishing (CMP) or grinding.

1 11. The method of Claim 1 wherein said interlevel  
2 dielectric has a thickness of from about 0.1 about 2.0  
3  $\mu\text{m}$ .

1 12. The method of Claim 1 wherein step (c) includes  
2 lithography and etching.

1 13. The method of Claim 1 wherein step (e) includes  
2 reactive-ion etching, ion-beam etching or plasma etching.

1 14. The method of Claim 1 wherein step (g) includes a  
2 deposition process.

1 15. The method of Claim 14 wherein said deposition  
2 process is selected from the group consisting of chemical

vapor deposition (CVD), plasma-assisted CVD, sputtering,  
plating and evaporation.

16. The method of Claim 1 further comprising a  
planarizing step after step (g).

17. The method of Claim 1 wherein between steps (f) and  
(g) a barrier layer is applied in said vias and spaces.

18. The method of Claim 1 wherein said vias are slot  
vias, stacked vias, standard vias or any combinations  
thereof.

19. The method of Claim 1 further comprising forming  
additional interconnect levels to said filled structure  
provided in step (g).

20. The method of Claim 1 further comprising repeating  
steps (a)-(g) any number of times to provide a multilevel  
interconnection structure wherein each successive level  
includes a patterned anti-fuse material formed thereon.

21. The method of Claim 1 further comprising forming a  
second interlevel dielectric layer on the structure  
provided in step (g), forming a tapered opening in said  
second interlevel dielectric level exposing the filled  
conductive vias and spaces; forming a second conductive  
material in said tapered opening; and reactive-ion  
etching said second conductive material.

22. An interconnect structure in which an anti-fuse  
dielectric is formed therein comprising:

3 a substrate having a first level of electrically  
4 conductive features;

5  
6 a patterned anti-fuse dielectric layer formed on said  
7 substrate, wherein said patterned anti-fuse dielectric  
8 layer includes an opening to at least one of said first  
9 level of electrically conductive features;

10  
11 a patterned interlevel dielectric material formed on said  
12 patterned anti-fuse dielectric layer, wherein said  
13 patterned interlevel dielectric includes vias, as least  
14 one of said vias has a via space formed above said  
15 opening; and

16  
17 a second level of electrically conductive features formed  
18 in said vias and via spaces.

1 23. The interconnect structure of Claim 22 wherein said  
2 substrate is composed of an interlevel dielectric  
3 material that is the same or different from said  
4 patterned interlevel dielectric material.

1 24. The interconnect structure of Claim 22 wherein said  
2 patterned interlevel dielectric material is composed of  
3 an inorganic semiconductor material selected from the  
4 group consisting of  $\text{SiO}_2$ ,  $\text{Si}_3\text{N}_4$ , diamond, diamond-like  
5 carbon and fluorinated doped oxides.

1 25. The interconnect structure of Claim 22 wherein said  
2 patterned interlevel dielectric material is composed of  
3 an organic dielectric material selected from the group

4 consisting of polyimides, polyamides, paralyene and  
5 polymethylmethacrylate.

1 26. The interconnect structure of Claim 22 wherein said  
2 first and second levels of electrically conductive  
3 features are composed of the same or different conductive  
4 metal selected from the group consisting of aluminum,  
5 tungsten, copper, chromium, gold, platinum, palladium and  
6 alloys, mixtures and complexes thereof.

1 27. The interconnect structure of Claim 22 wherein said  
2 anti-fuse dielectric layer is a dielectric material  
3 selected from the group consisting of  $\text{SiO}_2$ ,  $\text{Si}_3\text{N}_4$ , Si  
4 oxynitrides, amorphous Si, amorphous C, H-containing  
5 dielectrics, carbon, germanium, selenium, compound  
6 semiconductors, ceramics and anti-reflective coatings.

1 28. The interconnect structure of Claim 27 wherein said  
2 anti-reflective coating is silicon oxynitride.

1 29. The interconnect structure of Claim 22 wherein  
2 another interconnect level is formed over said patterned  
3 interlevel dielectric layer.

1 30. The interconnect structure of Claim 29 wherein said  
2 another interconnect level includes a tapered metal  
3 contact region.